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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/557,104	11/27/2006	Martin Heinen	20031035-02	5365

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EXAMINER	
CHARIOUI, MOHAMED	
ART UNIT	**PAPER NUMBER**
2857	

NOTIFICATION DATE	DELIVERY MODE
10/03/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

IPOPS.LEGAL@agilent.com

Office Action Summary	Application No.	Applicant(s)	
	10/557,104	HEINEN ET AL.	
	Examiner	Art Unit	
	MOHAMED CHARIOUI	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 July 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 February 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 7/14/08 has been entered.

DETAILED ACTION

Specification

2. The disclosure is objected to because of the following informalities: The Brief description of the drawings is missing. Appropriate correction is required.

Claim Objections

3. **Claim 12** is objected to because of the following informalities: Product is structure and is not possible to encode structure into a readable medium. The Applicant is encouraged to delete "or product" from the claim. Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Momtaz et al. (U.S. Patent Number 7,263,151) in view of Moll et al. (U.S Patent Number 7,069,488).

As per claims 1 and 10, Momtaz et al. teach a level comparator adapted for comparing a level of a comparator input signal with a comparison level and correspondingly providing a comparator output signal (see col. 2, lines 10-42), a sampling unit coupled to the level comparator and being adapted for sampling the comparator output signal (see col. 8, lines 50-56), and a bit error test unit adapted to receive the sampled comparator output signal and to determine therefrom an indication of a bit error in a sequence of the sampled comparator output signal (see col. 2, lines 10-25 and col. 3, lines 1-12).

Momtaz et al. fail to teach comparing the sampled comparator output signal against an expected pattern.

Moll et al. teach this feature (see col. 5, lines 8-21; col. 5, lines 49-55; col. 6, lines 2-21 and col. 6, lines 53-62). It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate Moll et al.'s teaching into Momtaz et al.'s invention because it would a deviation in the corresponding samples would indicate error in the signal. Therefore, accurate analysis of the signal would be performed.

As per claim 2, Momtaz et al. further teach a phase shifting unit being adapted to receive and phase-shift a clock signal and to provide to the sampling unit a phase-

shifted clock signal for controlling a sampling point of the sampling unit (see col. 2, lines 35-53 and col. 8, lines 50-56).

As per claims 3 and 11, Momtaz et al. further teach a control unit (e.g. delay circuit) being adapted to control at least one of the following: the phase-shifting of the phase shifting unit, the comparison level of the level comparator, operation of the bit error test unit (see col. 2, lines 35-43 and col. 8, lines 53-56).

As per claim 4, Momtaz et al. further teach that the controller is adapted to be controlled by at least one of the following: the bit error test unit (see col. 3, lines 1-12); an interface unit adapted to be coupled to a unit external with respect to the integrated circuit (e.g. interface in which data in are applied; see col. 4, lines 6-25 and Fig. 1).

As per claim 5, Momtaz et al. further teach an input unit (e.g. receiver 100, Fig. 1) adapted to receive an input signal from external with respect of the integrated circuit, wherein the input unit comprises: the level comparator adapted to receiving as the comparator input signal the input signal (comparator 114, Fig. 1), or a signal derived therefrom, and the sampling unit (see col. 4, lines 25-52 and col. 5, lines 15-23); a processing unit adapted to receive and process the sampled comparator output and an output unit adapted to receive a data signal from the processing unit to derive therefrom an output signal, and to provide the output signal to external with respect of the integrated circuit (see col. 2, line 53 through col. 3, line 12 and col. 3, line 64 to col. 4, line 25).

As per claim 6, Momtaz et al. further teach that the level comparator is adapted to provide at least one of the following: comparing the comparator input signal against a threshold value representing the comparison level (see col. 5, lines 32-38), comparing a normal signal (e.g. V_{BER}) of the comparator input signal against a complementary signal (e.g. V_{TH}) of the comparator input signal, with the complementary signal being complementary to the normal signal (see col. 3, line 66 through col. 4, line 24).

As per claim 7, Momtaz et al. further teach that the bit error test unit is adapted to provide at *least one of the following*: determining as the bit error indication *at least one of the following*: the number of bits in the sequence, the number of errors detected in the sequence, the number of error free bits in the sequence, *a value of a bit error rate representing the ratio of detected bit errors per number of bits* (see col. 3, lines 1-12 and col. 5, lines 24-50), determining the bit error indication with respect to at least one of the sampling point, representing a point in time relative to transition time of the clock signal, and the comparison level of the level comparator (see col. 4, lines 34-59), storing and/or buffering the bit error indication (see col. 3, lines 1-12), communicating the bit error indication to at least one of: another unit of the integrated circuit, a unit external with respect to the integrated circuit (see col. 5, lines 33-43).

As per claim 8, Momtaz et al. further teach an interface unit adapted to be coupled to an external bit error test processing unit being external with respect to the integrated circuit (see col. 2, lines 53-67), the interface unit being adapted to provide *at least one of the following*: communicating *at least one of status information of the bit error test unit and the bit error indication to the external bit error test processing unit*,

receiving a control signal from the external bit error test processing unit in order to provide at least one of: controlling operation of the bit error test unit, initiating operation of the bit error test unit, controlling operation of the control unit (see col. 5, lines 24-62).

As per claim 9, Momtaz et al. further teach the sampling unit comprises a deserializer (e.g. SONET OC-192) adapted for deserializing the comparator output (see col. 2, lines 53-67 and col. 4, lines 25-38), the integrated circuit further comprises a clock data recovery unit adapted to derive the clock signal from a data signal, preferably from one of: the comparator input signal, the input signal, a signal derived from the input signal, or the comparator output signal, wherein the phase shifting unit is coupled to the clock data recovery unit and receives the recovered clock signal therefrom (see col. 2, lines 35-52).

As per claim 12, Momtaz et al. further teach a computer readable medium encoded with a software program or product, for executing the method of claim 10 when run on a data processing system (see col. 3, line 44 trough col. 4, line 24).

As per claim 13, Momtaz et al. teach a level comparator adapted for comparing a level of a comparator input signal with a comparison level and correspondingly providing a comparator output signal (see col. 2, lines 10-42), a sampling unit coupled to the level comparator and being adapted for sampling the comparator output signal (see col. 8, lines 50-56), and a bit error test unit adapted to receive the sampled comparator output signal and to determine therefrom an indication of a bit error in a sequence of the sampled comparator output signal (see col. 2, lines 10-25 and col. 3,

lines 1-12), a processing unit adapted to receive and process the sampled comparator output signal (see col. 2, line 2 through col. 3, line 12).

Response to Arguments

5. Applicant's arguments with respect to claims 1-13 have been considered but are moot in view of the new ground(s) of rejection.

Contact information

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mohamed Charioui whose telephone number is (571) 272-2213. The examiner can normally be reached Monday through Friday, from 9 am to 6 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eliseo Ramos-Feliciano can be reached on (571) 272-7925. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Mohamed Charioui/

Examiner, Art Unit 2857

9/28/08